Multi-Source Data Oriented Flexible Real-time Information Fusion Platform on FPGA

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***Abstract*—To implement the algorithms of information fusion in industry, the DSP-FPGA hybrid system is usually used which combined the advantage of DSP and FPGA, easy programming and handling custom interfaces, together. However, the hardware of the hybrid system is relatively complex. In this paper, a new platform, which supports multiple inputs of sensors solely on FPGA, has been put forward. With the state-of-art SoPC (System on Programmable Chip) technology, our platform can integrate microprocessor and many interfaces of different sensors as logic circuits into FPGA so that the peripheral circuit and DSP can be simplified and even removed. Besides, the software development on the system can be implemented in C instead of HDL. The performance analysis is given and the system is proved to be a stable, cost-effective and power-efficient platform.**

Keywords- FPGA, Information fusion, SoPC, MicroBlaze

I. INTRODUCTION

Information fusion (IF) is to merge different information from multiple sources to one or fewer destinations. The sources are usually the sensors, database, and computers.[1][2] The aim of IF is to purify the different sources, preform redundancy, and inspect the main source. It is very important for critical systems of transportation vehicles, such as the safeguard and navigation systems of trains, vessels, and aircrafts.

In recent years, the information fusion is a hot topic for both industry and academia [3]. Many researchers have made their efforts to improve the algorithms of IF. However, fewer works are presented to provide the frameworks of real-time, highly integrated, stable platform for industry. [4]

To develop a system that can deploy IF algorithms, some requirements should be fulfilled. Firstly, the platform should support multiple inputs of sensors, further multiple interfaces with different protocols of interfaces, which is the basic and key property. Secondly, the process core on the platform should be flexible and easy enough to implement different algorithms. Finally, process core should have great computing power and the complex calculation of the tested algorithm can be finished in predictable time, which also mean real-time.

Taking the above three aspects into consideration, the industry usually exploits DSP-FPGA hybrid system. In this framework, the FPGA is performed as the interface chip to handle various protocols and gather data for DSP, while the DSP communicates with FPGA and is performed as core of processing. The advantage of this framework is that the FPGA can offer interfaces to multiple sensors for DSP and exploit its hardware level parallelism to accomplish the computing-intensive tasks such as protocol resolution, while the DSP controls all the data flows and perform the arithmetic operation. However, this solution enhances the difficulties of both the hardware circuits design and software development. The interconnections between DSP and FPGA are relatively complex and error-prone while the software applications are separated into two DSP part and FPGA part. More engineers will be needed which will increase the development costs.

To encounter these disadvantages, we propose our new architecture, as figure 1 shows. Compared with the hybrid system, the IF algorithms will be implemented in C language and run in MicroBlaze, a microprocessor in FPGA, which takes place of the role of DSP in traditional design and simplify both the hardware circuits and software development.

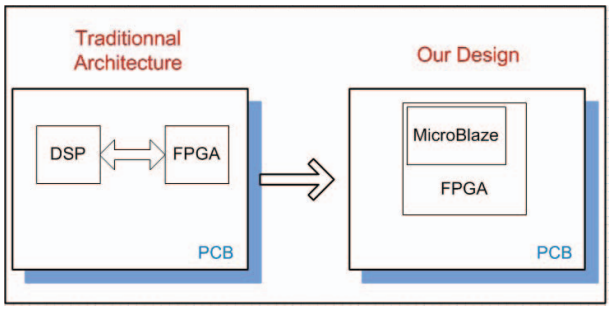

Figure 1. Comparation of two architectures

Our contributions lie in the following aspects. First, we propose a novel architecture with single FPGA to build the IF system. FPGA has flexible I/O configuration which make it feasible for design of multiple sensors' data path. The logic circuits in FPGA are programmable so that the configuration of system can be very flexible. Due to the hardware level parallelism, the computing power of FPGA makes the system meet the demand of real-time in data processing. Second, our design presents how to use the processor IP to prototype SoPC with FPGA. In our method, the software development and IF algorithm implementation will become much easier than the

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traditional FPGA development flow hence can shorten the development cycle [4][5][6].

The paper is organized as follows. Section 2 introduces the whole system and section 3 presents the hardware design. Section 4 explains how to develop the software and implement algorithm by using Xilinx tools. In section 5, the performance analysis is given in terms of stability, throughput and power consumption. Finally, section 6 concludes the paper.

II. SYSTEM OVERVIEW

The whole system architecture can be shown as figure 2. As in the figure, there are two parts in central FPGA: MicroBlaze as microprocessor and the peripheral IP cores. The peripheral circuits can be classified into different modules according to their variable functions. On the left side of the FPGA, they are the Phy interfaces which offer 100/1000Mbps speed. Also, the platform supports UART protocol such as RS422 and RS232. The parallel port consists of data path with 24 bits width bi-direction I/O and control path with 13 bits width output. Three components buildup the storage module: SPI Flash, Nor Flash and DDR2 SDRAM. The SPI Flash is used to store the hardware configuration and the Nor Flash is used to store the software runs on the MicroBlaze. During the run time, software runs in the DDR2 SDRAM.

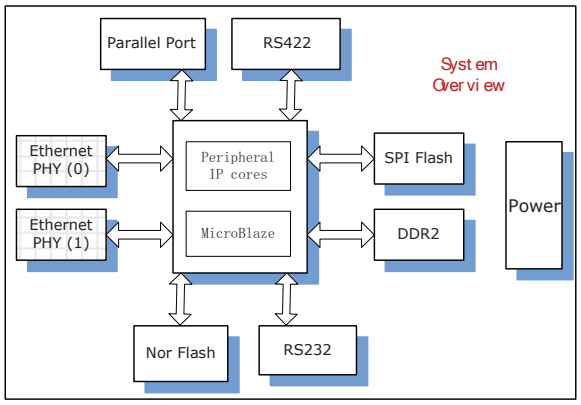

Figure 2. System Overview

In the logical level, the soft processor performs as the DSP in the hybrid system and the peripheral IP cores offer the interfaces. If needed, designers can instantiate more than one MicroBlaze processors. The only limitation is that chip resources (e.g. LUTs, slice and Block Ram) can restrict the overall configuration of circuits. Xilinx provide an "Embedded Development Kit" to deploy the software application written in C language. After cross-compiling, the binary code can run in MicroBlaze processor to control the peripheral hardware.

III. HARDWARE DESIGN

Before designing the Printed Circuits Board (PCB), it's important to define system functions, verify the feasibility of design, put forward the possible performance and estimate the costs. After all have been done, the FPGA should be chosen according to the demands as well as considering development maturity and the number of I/O pins. Then all the possible types of FPGAs can be decided. The electrical characteristics and working temperature are two main properties in choosing the precise models and the chips must be easy to buy. After all chips of the system are decided, the system hardware and circuits design can be done with the guidance of corresponding data sheet. In the following chapter, the FPGA minimum system is introduced first and then the communication interface. The former part is the core required by any FPGA system design and the latter is unique in our design.

A. FPGA Minimum System

FPGA minimum system refers to the basic circuits that the FPGA can work independently as the process core [6]. Commonly, the minimum system is divided into several parts. They are FPGA I/O, clock, power and configuration circuits.

The FPGA chip of our prototype is from the Spartan-6 family providing leading system integration capabilities with the lowest total cost for high-volume application. The clock is provided by a 100MHz crystal. The Table I. shows the detailed resources [7].

TABLE I. DEVICE RESOURCES

Device	Logic Cells	Configuration Logic Blocks		
		Slices	Flip-Flops	Max Distributed RAM
XC6SLX45	43,661	6,822	54,576	401
Device	**DSP Slices**	**Block RAM Blocks**		**CMTs**
		18Kb	**Max(Kb)**	
XC6SLX45	58	116	2088	4

The platform is provided with a 5v outside power supply. However, the voltages of whole system varied from 1.2v to 5v. For Spartan-6 FPGA, the Vccint is set to 1.2v and the Vccaux is set to 2.5v. The FPGA's four I/O banks are set to 1.8v. The two ethernet chips require 2.5v and the DDR2 needs both 1.8v and 0.9v voltage. Besides, the UART ports needs optoelecric coupling and isolated DC/DC converter. All the different voltages can be gained from different power management ICs.

The configuration circuits are the connection between software design and the hardware platform. The configuration data or "bitstream" will be erased after the FPGA power down. So it should be stored into external memory and loader to the FPGA whenever the power is on. We use three ways to configure the FPGA: JTAG, SPI model and BPI model [9]. The SPI Flash, which stores bitstream, is used in SPI model while the Nor Flash is used in BPI model, which store software program in the format of MCS. The DDR2 stores software code and data in run time. After power on, the FPGA reads the bitstream from the SPI Flash. Usually the software program is bigger than the SPI Flash so that it has to be stored in the Nor Flash. In the SPI Flash, there is bootloader program which is designed to carry code and data of the software from Nor Flash to DDR2 SDRAM. Finally, the program will run in SDRAM.

B. *Communication Interface*

The communication interface refers to the UART ports, Ethernet interfaces, the parallel ports and other type of ports. These interfaces determine the communication ability of the platform with different sensors. So the design of the communication interface is a key point for the whole system. The communication methods and protocols of sensors can be classified into four categories: UART port, Ethernet interface the parallel port and user-define port.

The "UART" is the most common serial communication method between host machine and guest machine or between computer and the sensors. The standards protocols for UART are EIA RS-232, RS-422 or RS-485. The UART is easy to generate high voltage due to long transmission line so the protective isolation is needed. The basic idea is that the protective isolation module can separate the component which is easy to be damaged by the high voltage from the main system and avoid physical connection between them. The signal transmission is usually accomplished by photo coupling or electromagnetic coupling.

The Ethernet is a kind of computer networking technology for data communication. In the standard networking model, the Ethernet has defined the wiring and signal standards for the Physical Layer and the lower part of the "Data Link Layer". In our design, the Ethernet ports support both 100/1000M and are self-adaptive.

The parallel port is used by the RDC module such as the brushless resolver and differential synchrony. The platform has a 24 bits-width data path and 13 bits-width control signal path. The data path is bi-direction and the control signal is only output. Due to the FPGAs' limited driving capacity, the voltage should be shifted from 3.3v to 5v which can also increase the current driving capacity. By assert different control signal, the parallel port's direction will change to input, output or just high-impedance.

IV. SOFTWARE DESIGN

SoC, which means System on a Chip, refers to integrating all components of a computer or other electronic system into single integrated circuit or chip [10]. Its excellent performance lies in size, costs, stability and power efficiency. Normally, the SoC is built as ASIC which may contains fixed digital, analog, mixed-signal functions. SoPC means programmable SoC whose components and functions can be changed according to the demands of the developer. That is to say SoPC is more flexible than SoC. More important, the developing on SoPC, which is based on C language, is quite different from the traditional FPGA, which is based on HDL such as Verilog or VHDL. Thus the development cycle can be shortened and the degree of difficulty can be decreased. Combined with the reconfigurable ability of FPGA, the concept of SoPC attracts engineers and researchers' attention.

A. *Development Flow*

Embedded design in an FPGA consists of the following steps [11]:

1. Generate BSP and Netlist through EDK
2. FPGA hardware design
3. Embedded software application development
4. Create the download bitsream

The figure 3 shows the exact development flow.

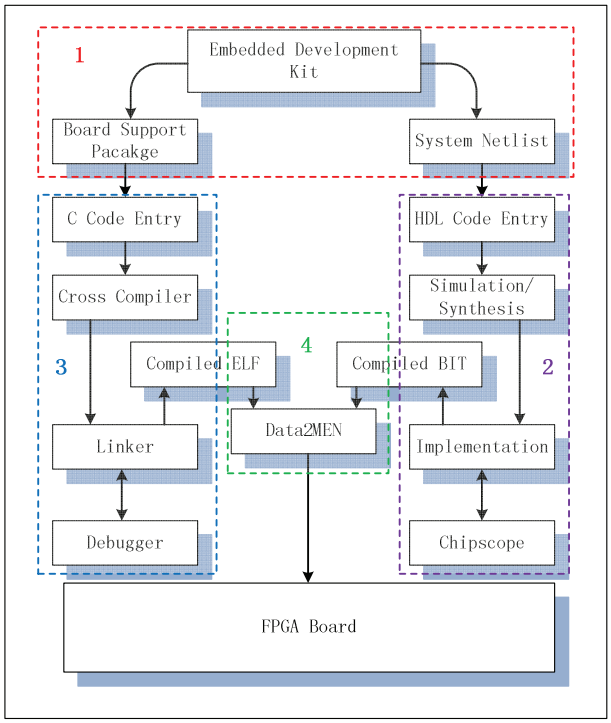

Figure 3. Diogram of Embedded Design Flow on FPGA

B. *Xilinx Tools*

The Xilinx's "Embedded Development Kit" is a collection of all necessary tools, documentation and IP for build SoPC on Xilinx product [12]. According development flow introduced above, we will briefly describe the tools integrated in EDK. In the first step, the embedded hardware should be developed. The EDK will assist users to build the custom hardware platform by "BSB"(Base System Builder). Then the "PlatGen" will generate HDL netlist. When the hardware flow is done, the user can develop the software in SDK. In SDK, the libraries and drivers is generated from the "LibGen". The code is usually written in C which is familiar to many engineers and easy to learn and easy to use. Through the crossed compiler, the application for the platform will be generated by the host machine. The "XMD" and GNU are both good debug tools. Finally, the EDK combined the ELF and bitstream together and download them to the target board using "iMPact".

V. PERFORMANCE EVALUATION

To evaluate a digital system's performance, there are three aspects should be commonly considered: stability, throughput and power consumption. Considering the functions of our platform, it is equal to an integrated system such as industry personal computer (IPC) with a multi-serial-port card, a

parallel port card, two network cards and a CPU card or a DSP-FPGA hybrid system. In this section, we compare the platform with IPC and DSP-FPGA hybrid system in three aspects.

A. Stability

Stability is the most important factor when evaluate the system performance. Since digital system is connected by different parts so that all the components should work together, the breaking down of any part can lead to the crash of whole system. To achieve the interconnection, the IPC should have a mother board which contains multiple PCI slots to infix all the cards. For DSP-FPGA system, the connecting finger between the cards and the PCI slots are instead of interconnection in the PCB which increases the robustness of the system. But in our solution, most of the logic circuits have been integrated into the FPGA which means even less off-chip connection than the DSP-FPGA system. Meanwhile, the circuits also have been simplified so as to make it possible to be more stable when working under more severe environment.

B. Throughput

Throughput is total number of date that successfully processed or delivered by the system. Generally, higher throughput means better performance because with higher throughput, the system can support more work load. Usually, for digital system, the bottle-neck of the throughput comes from the limited I/O capacity. It's obvious that the IPC has the highest I/O capacity while our SoPC solution is the lowest. So it seems that the throughput of IPC is higher than our solution.

However, for information fusion platform, it's not the truth. The computing power rather than I/O capacity becomes the bottle-neck of the whole system. The communication speed of the sensor is usually very slow. For instance, the UART commonly send data with the Baud rate of 9600 or 4800 which is quite a low speed. Due to the limitation of the process ability of DSP, the IPC's high I/O capacity is wasted. In our solution, the specific hardware-based algorithms may be encapsulated as IP core to promote the performance. Also, the developer can allocate multiple MicroBlaze processors if need under the constraint of on-chip resources. For instance, a MicroBlaze processor runs at 111MHz need 2447 LUTs[13]. XC6SLX45 has 6,822 slices which means 27288 LUTs. The designers can build a multiple processors system contains as much as 10 MicroBlaze processors. So our platform has high throughput than the other two solutions.

C. Power Comsuption

Reducing the power consumption can benefit to two aspects: First, with lower power consumption, the system can work longer with the same energy, which is very important for embedded system using battery as power. Second, the decrease of the consumption will cut the amount of heat produced by the system. Compared with the IPC, it's not necessary to install fans for thermal dissipation. Only a heat sink is need which can even save power for the fan and reduce the noise.

TABLE II. POWER CHIPS CAPACITY

Output Voltage	**5v**	**3.3v**	**2.5v**	**1.8v**	**1.2v**	**0.9v**
Output Power	4w	1.25w	1.25w	1.5w	1.25w	1.73w

Table II shows the power consumption of our platform. All the output power is the maximum output value in datasheet. Actually, the power consumption during run-time might be lower than this. The maxim power consumption is 11w in total while the IPC is over 100w. Since there are only FPGA on the PCB and the circuits have been integrated in the FPGA, the power consumption is also lower than DSP-FPGA hybrid system which is about 30w.

VI. CONCLUSION

The paper introduces a novel architecture for information fusion platform. Using FPGA as the central unit, the whole system can meet the demands of IF algorithms which are usually computing-intensive tasks. The SoPC technology offers a new method to build the embedded system and simplify the development of digital product on FPGA. With multiple sensor interfaces, the platform not only provides a chance to evaluate IF algorithm in real environment, but also can be used for industry uses such as multi-sensor-port card or navigation computer which is connected to many sensors as the core of the navigation system. The platform is stable, low-cost and power efficient for both research and industry use with real-time processing ability and high flexibility.

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